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L3	0	((((force or forced or forcing) with node) and ((release or released or releasing) with node) and ((monitor or monitored or monitoring) with node)) and (hdl or vhdl or verilog)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/02/09 14:07
L4	9	((((force or forced or forcing) with node) and ((release or released or releasing) with node)) and (hdl or vhdl or verilog)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/02/09 14:08
L5	21	((((force or forced or forcing) with signal) or ((release or released or releasing) with signal)) and (hdl or vhdl or verilog) and (initial with node)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/02/09 14:12
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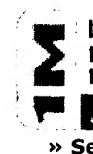
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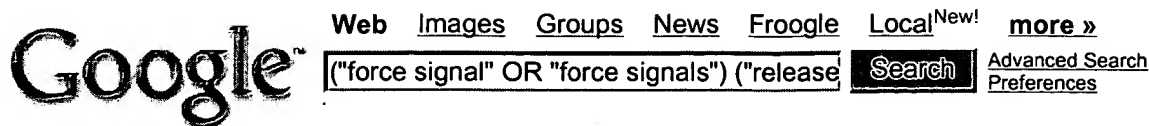
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... The system task \$finish is executed from the **Verilog** source. The user presses the keystroke `Ctrl-\' ... **force** <signal> <dboh>. ... **release** <signal>. ...

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... display the value of a signal similar to \$display. **force** <signal> <dboh>. ... **release** <signal>. ... Execute a task defined in the **Verilog** source code. ...

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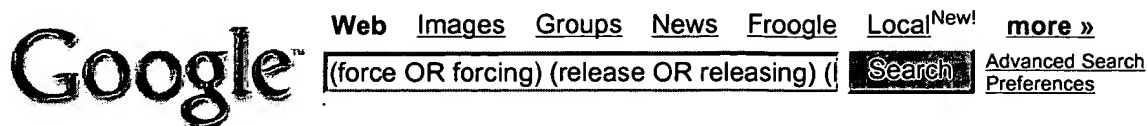
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... I expect this program to replace the **verilog.sh** script before the 0.3 **release**.

And *finally* I got started on **force/release**. In fact, **force** assignments ...

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... in QuickWorks (as well as other third-party **Verilog** and **VHDL** simulators) ...

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... **release** from last year used as digital engine for Antrim **Verilog**-AMS simulator

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... D flip-flop but reset **_L** should be implemented with **force/release** state- ...

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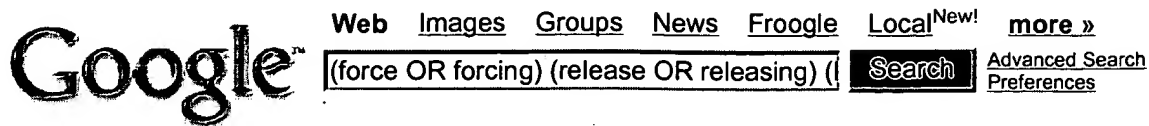
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... **Force**, **release**, and hierarchical net names (these are used for ...

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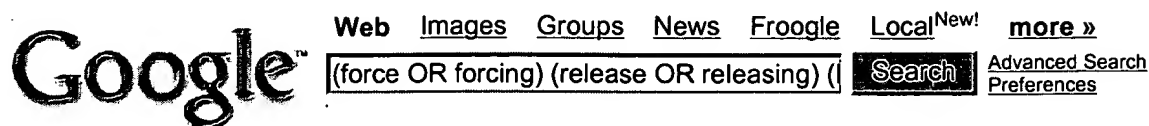
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